**AMENDMENTS TO THE DRAWINGS:**

The attached two (2) replacement Sheets of drawings include changes to Figs. 1 to 2. The Replacement Sheets, which include Figs. 1 and 2, replace the original two sheets including Figs. 1 and 2. In Fig. 1, descriptive text labels for various boxes have been added. In Fig. 2, the descriptive text labels have been replaced with English translations as follows:

Adresse -> Address

Zeilenindex -> Line Index

Zeile -> Line

Wort -> Word

Byteanwahl -> Byte Selection

Zeilenanwahl -> Line Selection

Daten -> Data

Zeilendecodierung -> Line Decoding

Gültige Daten -> Valid Data

Von / zum Datenbus -> To/From Data Bus

No new matter has been added, and the Replacement Sheets are supported by the present application, including the specification.

Attachments: two (2) Replacement Sheets

## REMARKS

### I. Introduction

With the cancellation of claim 19, claims 15-18 and 20-28 remain pending and rejected in the present application. Claims 15, 20, 21 and 27 have been amended. For at least the reasons set forth below, Applicants respectfully submit that the claims are in condition for allowance.

### II. Objections to the Drawings

Figures 1 and 2 have been redrawn to include English descriptive text labels and for clarity. In addition, the Specification has been amended to delete the reference "ff," rendering moot the objection to the drawings concerning this reference. Withdrawal of the objections to the drawings is respectfully requested.

### III. Objection to the Specification

The Examiner has objected to the use of the terms "n-of-m" and "1 of K" in the Specification. As described in page 2, lines 8 to 10, n and m are natural numbers, with m being greater than 2 and n being greater than m/2. An n-of-m code, which is alternatively known as an m-of-n code, is a known error detection code in which the total number of occurrences of a value is checked. In this case, it is checked whether the value has occurred n times out of a maximum possible m times. Similarly, "1 of K" means the value is checked to see if it occurs once out of K times. Since these terms would be clearly understood by one of ordinary skill in art – especially in view of the Specification –, withdrawal of the objection to the Specification is respectfully requested.

### IV. Rejection of Claims 15-28 under 35 U.S.C. § 102(e)

Claims 15-28 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,345,582 ("Tsuchiya"). Applicants respectfully submit that Tsuchiya fails to anticipate pending claims 15-28, for the reasons explained below.

To anticipate a claim under § 102(e), a single prior art reference must identically disclose each and every claim element. See Lindeman Machinenfabrik v. American Hoist and Derrick, 730 F.2d 1452, 1458 (Fed. Cir. 1984). If any claimed element is absent from a

prior art reference, it cannot anticipate the claim. See Rowe v. Dror, 112 F.3d 473, 478 (Fed. Cir. 1997). Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claim invention, arranged exactly as in the claim. Lindeman, 703 F.2d 1458 (Emphasis added). Additionally, not only must each of the claim limitations be identically disclosed, an anticipatory reference must also enable a person having ordinary skill in the art to practice the claimed invention, namely the inventions of the rejected claims, as discussed above. See Akzo, N.V. v. U.S.I.T.C., 1 U.S.P.Q.2d 1241, 1245 (Fed. Cir. 1986). To the extent that the Examiner may be relying on the doctrine of inherent disclosure for the anticipation rejection, the Examiner must provide a "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flow from the teachings of the applied art." (See M.P.E.P. § 2112; emphasis in original; see also Ex parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)).

Claim 15 has been amended herein without prejudice to include the features of canceled claim 19. Amended claim 15 recites, in relevant part, "**storing a valid-invalid bit at least in duplicate in the cache memory**." Amended claim 27 recites substantially similar features as the above-recited features of claim 15.

The Examiner contends the above-recited features are disclosed in col. 5, lines 43-65 of Tsuchiya. However, the cited section only refers to the detection of cache errors, the occurrence of which is indicated by the output of a series of AND gates, e.g., the AND gate 72. The error-indicating output is not **stored in the cache**, but instead transmitted externally through a corresponding set of output lines. Further, it is readily apparent that the error indicated by the output is not analogous to a **valid-invalid bit**. The concept of validity in the context of a memory cache is well understood, i.e., validity of a specific memory content inside a cache refers to the condition in which the memory content is expected to contain the most recent and correct data value for the memory location being cached. The error indicated by the output in Tsuchiya, while indicating errors such as a cache miss, an address parity error, or a data parity error, does not indicate the validity of the data contained in a specific cache location.

For the foregoing reasons, claims 15 and 27, along with dependent claims 16-18, 20-26 and 28, are not anticipated by Tsuchiya. Withdrawal of the anticipation rejection of pending claims 15-18 and 20-28 is respectfully requested.

Independent of the above, claim 23 recites, in relevant part, "**comparing the first line index to a second line index applied at the cache memory; and retrieving the first line index from the cache memory by line decoding**." The Examiner contends that this feature is disclosed in Figure 2 of Tsuchiya. However, it is unclear where the feature of **line decoding** is shown. The recited feature refers to the detection of errors by **back-decoding** of a selected line and **comparison** of the address retrieved from it to the selected line index. This comparison is shown by the comparator V1 in Figure 2 of the present application. In contrast, Tsuchiya refers to the reading out of parity bits stored in the cache, but fails to even suggest the back-decoding and comparison provided in claim 23. Accordingly, claim 23 and dependent claims 24 and 25 are allowable for these additional reasons.

## V. Conclusion

In view of the foregoing, it is submitted that claims 15-18 and 20-28 are in allowable condition. It is therefore respectfully requested that the present application issue as early as possible.

Respectfully submitted,
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